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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/207,745	12/08/1998	DANIEL S. SIMPKINS	32172-143271	7213

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EXAMINER	
TRAN, PHUC H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/207,745	Applicant(s) SIMPKINS ET AL.	
	Examiner PHUC H TRAN	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,21-26 and 28-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,21-26,28-53,55,56 and 62* is/are rejected.

7)☒ Claim(s) *54 and 57-61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 13,21-26,28-62 are objected to because of the following informalities: "**single** shared memory" is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Appropriate correction is required.

2. Claims 13, 21, 31, 34, 35, 41,& 50 are objected to because of the following informalities: "storing the TDM data in a single memory **based on a time slot of a frame**" is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Appropriate correction is required.

3. Claim 21, 35, and 41 are objected to because of the following informalities: "a time slot interchange controller coupled to said single shared memory to **select addresses** in said single shared memory **to store TDM data**, said time slot interchange controller to **select an address of said single shared memory** for a TDM data **based on a time slot of a frame**" is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Appropriate correction is required.

4. Claims 54, 57, & 61 are objected to because of the following informalities: "said time slot interchange controller **selects a same address for single shared memory**" is not described in the specification in such a way as to reasonably convey to one skilled in

the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 60 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regard to claim 60, "said TDM memory portion accommodates NxM TDM data" is not described in the specification in such a way as to reasonable convey to one skilled in the art.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 13, 21-26, 28-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Kosuge et al. (U.S. Patent No. 4575844).

- With respect to claims 13, 21, 31-35, 41, 48-53, 55-56, & 62, Kosuge teaches a switch for switching time division multiplexed data and packet data from input ports to output ports (e.g. Fig. 1 shows the basic system configuration of a digital switching system for circuit and packet through TDM), which comprises:

a plurality of input ports receives data (e.g. terminals in Fig. 1), wherein each data comprises either TDM data or packet data (e.g. the line 15 shows the TDM input data in Fig. 1 and Fig. 7);

a plurality of output ports transmits switched data (e.g. terminals in Fig. 1);

and a single shared memory (e.g. hierarchical storage in Fig. 1) couples the input ports to the output ports (to the multiplexer in Fig. 7), the shared memory sequentially receives all TDM data and packet data from the input ports (e.g. the shared memory sequences receiving in input line 15); the single shared memory stores both TDM and packet data; the single shared memory switching all sequentially receives TDM and packet data from respective input ports to respective output ports (e.g. the shared memory sequences outputting data on output line 16), wherein switching of packet data by the single shared memory has neither latency nor jitter effect on switching of TDM data by the single shared memory (see col. 1, lines 64-67 and Fig. 5) and wherein switching of TDM data is based on input time slots of the TDM data (Fig. 3b);

a time slot interchange controller couple to the single shared memory selecting address in the single shared memory to store TDM data (CKT switching call program in Fig. 6), the time slot interchange controller selecting an address of the single shared memory to store for a TDM data based on a time slot of a frame in which the switch

received the TDM data (CKT switching call program control the CKT switching call buffer for transmit data, Fig. 7, Fig. 11);

and a packet switch controller coupled to the single shared memory selecting address in the single shared memory to store packet data (packet switching call program), the packet switch controller selecting an address of the single shared memory for a packet data based on routing data embedded in the packet data and based on the input which received the packet data (Fig. 7, Fig. 12, col. 2, lines 11-26). Kosuge explicitly fails to teach the time slot interchange controller, but it is inherently to understand the switching programs circuit/packet is for controlling of transmission in time slot.

- With respect to claims 22 & 36, Kosuge explicitly fails to teach each data is received by an input port as a time slot in a frame, but it inherently know the TDM comprising time slots, which assigns a fixed number of bits in each frame.

- With respect to claims 23, 37, & 42 Kosuge further teaches the single shared memory, which comprises a TDM data memory portion (e.g. CKT switching call buffer in Fig. 1) and a packet data memory portion (packet switching call buffer in Fig. 1).

- With respect to claims 24, 38, & 43, Kosuge discloses the single shared memory that treats the input ports as logical input ports (e.g. the input port in Fig. 1 as terminals).

- With respect to claims 25, 39 & 44, Kosuge teaches the single shared memory places sequentially received packet data in a queue for a respective output port (e.g. data is received at the switch memory to transmit to the output).

- With respect to claims 26, 40, & 45-46, Kosuge also teaches the input ports receive the data and transmitted by the output ports as data exchange units (e.g. the

system of Kosuge utilizes the TDM with time frame as exchange unit to transmit data from input to output port).

- With respect to claim 28, Kosuge explicitly fails to teach the switching of a data from a respective input port to a respective output port is controlled by a stored switch configuration, but it is inherently to know the control section 14 in Fig. 1 for control the switching of data from input to output.

- With respect to claims 29 & 47, Kosuge also teaches an input data router sequentially routing data from the input ports to the single shared memory; and an output data router sequentially routing data from the shared memory to the output (e.g. Fig. 1 shows the sequentially routing data from the input to the shared memory and to the output).

- With respect to claim 30, Kosuge discloses wherein the data are received by input ports and transmitted by the output ports as data exchange units (e.g. the system of Kosuge as exchange unit to transmit data from input to output port). The data exchange units for packet data comprise routing information (e.g. the digital switching units 10 in Fig. 1 are for routing information from one terminal to another). The stored switch configuration uses the routing information of data exchange units for packet data to determine respective output port to switch the data exchange units (e.g. the control section is for controlling and routing the information through the digital switch unit). Kosuge explicitly fails to discloses the switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration, but it inherently understand the control section 14 in Fig. 1 for control the switching of data from input to output.

Allowable Subject Matter

9. Claims 54, 57- 59 and 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim 60 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments filed 5/6/04 have been fully considered but they are not persuasive.

- It's noted in Applicant's remarks indicated that the memory in Kosuge is not a single shared memory. Examiner respectfully disagrees with Applicant. Kosuge teaches a single shared memory as Hierarchical storage, which has many portions such as small, large capacity memory and file memory; therefore, the hierarchical storage is considered as the single shared memory for storing data. In Fig. 7 of Applicant shows the single shared memory, which includes packet data memory and TDM data memory, therefore the Kousuge's memory is like the memory in Fig. 7.

- Applicant's argument that Kosuge fails to teach storing the TDM data in a single shared memory based on a time slot of a frame. Examiner respectfully disagrees. In col. 6, lines 1-30, Kosuge teaches steps of input/output corresponding to time slot or cycle. Therefore the share memory stored data or read data based on cycle or time slot.

- Applicant's argument that Kosuge fails to teach a packet switch controller to select an address of a single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Examiner respectfully disagrees. Kosuge teaches the system mapping the virtual address space in the memory (Fig. 9, see bridge paragraph between col. 8-9)

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUC H TRAN whose telephone number is (703) 308-7471. The examiner can normally be reached on M-F (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RAO SEEMA can be reached on (703) 308-5463. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 872-9314.

Phuc Tran
Assistant Examiner
Art Unit 2664

P.t
July 23, 2004

DANG TON
PRIMARY EXAMINER